CLAIMS

That Which Is Claimed:

1. A linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time approach, comprising the steps of:

computing first and second stages of $\log_2 N$ stages of an N-point FFT/IFFT as a single radix-4 butterfly operation while implementing the remaining ($\log_2 N$-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops; and

distributing the butterfly operations in each stage such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

2. A linear scalable method as claimed in claim 1 wherein said step of distributing butterfly operations is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

3. A linear scalable system for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time approach, comprising:

means for computing first and second stages of $\log_2 N$ stages of an N-point FFT/IFFT as a single radix-4 butterfly operation while implementing the remaining ($\log_2 N$-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops; and

means for distributing the butterfly operations in each stage such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

4. A linear scalable system as claimed in claim 3 wherein said means for distributing the butterfly operations is implemented by means for assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

5. A computer program product comprising computer readable program code stored on a computer readable storage medium embodied therein for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time approach, comprising:

computer readable program code means configured for computing computing first and second stages of $\log_2 N$ stages of an N-point FFT/IFFT as a single radix-4 butterfly operation while implementing the remaining ($\log_2 N$-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops; and

computer readable program code means configured for distributing the butterfly operations in each stage such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

6. The computer program product as claimed in claim 5 wherein said computer readable program code means configured for distributing the butterfly operations is implemented by computer readable program code means configured for assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.